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JC955 U.S. PTO 11/03/00

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 003242.P015 Total Pages 2

First Named Inventor or Application Identifier Jean-Didier Allegrucci

Express Mail Label No. EL672752451US

ADDRESS TO:	**Assistant Commissioner for Patents** **Box Patent Application** **Washington, D. C. 20231**

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 13)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 3)

4. ____ Oath or Declaration (Total Pages ___)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. _____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))

9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)

_____ b. Power of Attorney

10. _____ English Translation Document (if applicable)

11. _____ a. Information Disclosure Statement (IDS)/PTO-1449

_____ b. Copies of IDS Citations

12. _____ Preliminary Amendment

13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)

14. _____ a. Small Entity Statement(s)

b. Statement filed in prior application, Status still proper and desired

15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. X Other: Certificate of Express Mail with copy of postcard showing contents of Express Mail package.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: _____

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)

or

X Correspondence Address Below

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PTO/SB/17(6/99)
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FEE TRANSMITTAL FOR FY 2000

TOTAL AMOUNT OF PAYMENT ($) 710.00

Complete if Known:
Application No. Not yet assigned
Filing Date Herewith
First Named Inventor Jean-Didier Allegrucci
Group Art Unit Not yet assigned
Examiner Name Not yet assigned
Attorney Docket No. 003242.P015

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

Deposit Account Number 02-2666
Deposit Account Name

[X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

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2. X **Payment Enclosed:**
X **Check**
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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility application filing fee	710.00
106	310	206	155	Design application filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 710.00

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	18	– 20** =	0	X 18.00	= .00
Independent Claims	3	– 3** =	0	X 80.00	= .00
Multiple Dependent					=

**Or number previously paid, if greater; For Reissues, see below.

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $_____

Patent fees are subject to annual revisions. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid.
See Forms PTO/SB/09-12

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,210	241	605	Petition to revive unintentionally abandoned application	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	690	249	345	For each additional invention to be examined (see 37 CFR 1.129(a))	
				Other fee (specify) _____	
				Other fee (specify) _____	

SUBTOTAL (3) $_____

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: Tom Van Zandt

Signature _____ Date _____

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Attorney Docket: 003242.P015 *PATENT*

UNITED STATES PATENT APPLICATION

FOR

DIAGNOSTIC SCHEME FOR PROGRAMMABLE LOGIC IN A CONFIGURABLE SYSTEM ON A CHIP

First Named Inventor:

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DIAGNOSTIC SCHEME FOR PROGRAMMABLE LOGIC IN A SYSTEM ON A CHIP

FIELD OF THE INVENTION

The present invention relates generally to diagnostic methods for programmable logic, and more specifically to accessing programmable logic in a system on a chip bus-based system.

BACKGROUND

A recent development in micro-electronics is the configurable system on a chip (CSOC). The system integrates a CPU, an internal system bus, and programmable logic, also referred to as configurable system logic (CSL). The various system resources are all interconnected, and communicating through an internal system bus, on a single piece of silicon. The internal system bus signals and various dedicated system resource signals that connect to the CSL are collectively referred to as the configurable system interconnect or CSI. There are two types of pins, dedicated pins to interface with external devices (e.g., external memory) and programmable pins that can serve as an interface to other user logic. The dedicated processor bus and system resources provide an efficient and stable high performance system, while the configurable system logic provides flexibility for the user to implement additional functions. There are many benefits to embedding the programmable logic, including time-to-market, integration, and flexibility. The downside of embedding the programmable logic is that the signals are not directly accessible (i.e., observable and controllable) by the engineer charged with system debugging. Many of the signals that are of considerable interest when debugging a system are now buried inside the device. As a result, system debugging and trouble-shooting capability can be severely limited.

SUMMARY OF THE INVENTION

A method is described for diagnosing programmable hardware in a programmable logic system. The method comprises ceasing bus access upon the occurrence of a specified event or sequence of events while allowing the completion of all pending transactions. When all pending transactions are completed the system clock is stopped such that the state of the programmable hardware is held static. The static state of the hardware is then accessed through a debug port. An apparatus and a machine readable medium that implement the method are also described.

Other features and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

Figure 1 is a block diagram of a configurable system on a chip;

Figure 2 is a timing diagram for the clock freeze operation; and

Figure 3 is flow chart of the clock freezing process of an embodiment of the present invention.

DETAILED DESCRIPTION

An embodiment of the present invention will provide a more efficient method of debugging user-implemented hardware in a configurable system on a chip. An embodiment of the invention allows the user to freeze the clock upon the occurrence of a user-specified event while avoiding the possibility that the clock will be frozen in a wait state. In one embodiment of the present invention the breakpoint unit of the system is programmable and will issue a clock freeze event upon the occurrence of a programmed event or sequence of events. The bus arbiter will cease granting bus access at this time, but will allow all pending transactions to be completed. The system can be stopped and the state of the system at a particular point can be viewed for debugging purposes. This method provides the user with a "snapshot" of the system at a desired time.

An intended advantage of one embodiment of the invention is to provide the user with the state of the system at a given time for debugging purposes. Another intended advantage of one embodiment of the invention is to ensure that the system is not currently in a wait state when the system clock is stopped. This allows the bus to be used by the debugging port.

Figure 1 is a block diagram of a configurable system on a chip. The system 100 shown in Figure 1 includes those portions of a CSOC relevant to an embodiment of the present invention, although a variety of different computing systems can implement the present invention. The system 100 shown in Figure 1 includes a configurable system logic 105, which is coupled to the rest of the system through the configurable system interconnect 110 CSI. The rest of the system 125 includes the CPU, DMA, peripherals, counters, timers, memory, and memory interfaces. The system includes a debug joint test action group (JTAG) port 115 that is connected to

a user input device 120 that is external to the chip, for example, a computer. The debug JTAG port 115 is a busmaster on the CSI bus 110 and therefore has access to any resources connected to the CSI bus 110. This includes the breakpoint unit 130, so that the user can program the breakpoint unit 130 through the JTAG port 115. In one embodiment the breakpoint unit 130 connects to, and allows tracing of, multiple buses and includes the ability to break on the occurrence of a predetermined bus event on any one of the multiple buses. In one embodiment the breakpoint unit 130 may be connected to, and programmed by, a host debugging system via a port on the target chip.

The breakpoint unit monitors the CSI bus 110. The user programs the breakpoint unit 130 to break on a specific condition or sequence of events. The breakpoint unit 130 may be configured to generate one or more output signals upon a breakpoint event. The output signals may be used to interrupt of freeze a processor, depending on the processor's supported features. So, for example, the user may program the breakpoint unit 130 to break as soon as there is a write to a specific register address. As soon as that happens, the breakpoint unit 130 generates a breakpoint event (e.g., the breakpoint unit 130 generates a clock freeze cycle). The clock freeze signal is propagated to the system clock. However, due to the pipeline nature of the bus, there may be pending operations from the bus that are being executed. For example, before the write signal that triggered the breakpoint there may have been a read that was being executed. That read may be to an external memory device that takes several cycles to execute and may, therefore, be in a wait state. There could be many other examples of accessing something in the configurable system logic that might have generated a wait state prior to the breakpoint event. All of these transactions must be terminated prior to freezing the

clock. If the transactions were not completed the system might be frozen while in a wait state, which would render the CSI bus 110 inoperable. The bus arbiter 135 is monitoring the CSI bus 110. In one embodiment the bus arbiter 135 is a state machine that implements a round-robin arbitration algorithm. One function of the bus arbiter 135 is to receive access requests from the several bus masters and grant access to a particular bus master after each clock cycle based on the arbitration algorithm. Another function of the bus arbiter 135 is to keep track of all transactions on the CSI bus 110 for debugging purposes. When the bus arbiter 135 receives a clock freeze signal from the breakpoint unit 130, the bus arbiter 135 stops granting access on the CSI bus 110. The bus arbiter 135 then waits for pending transactions to be completed and then allows the clock to be frozen, because only at this point can it be guaranteed that there won't be any wait states generated and that's because there are no more transactions pending on the bus.

Figure 2 is an example of a timing diagram for the clock freeze operation discussed above in reference to Figure 1. At T_0 Figure 2 is an example of a waveform diagram for the clock freeze operation discussed above in reference to Figure 1. The system clock 205 is functioning, the CSL clock 220 is functioning and therefore any requests, for example a DMA bus request 225, is granted. The DMA grant signal 230 is high, indicating that requests, for example DMA request 225, are being granted. At some time, T1, a clock freeze event occurs and the clock freeze event 210 goes high. At this point the arbiter stops granting any requests. The DMA grant line 230 goes low, indicating that no CSI requests will be granted. However, the qualified clock freeze signal 215 remains low, and remains low until some time, T3, where the last pending transaction is completed. The bus arbiter is aware of the last pending transaction completion. When the last pending transaction is complete

the bus arbiter transmits the qualified clock freeze signal, and qualified clock freeze 215 goes high. The qualified clock freeze signal freezes the CSL clock as indicated by CSL clock signal 220 which stays high during the debugging process.

Figure 3 describes the process by which the clock is frozen accordance with one embodiment of the present invention. Process 300 shown in Figure 3 begins at operation 305 in which a breakpoint event occurs. The breakpoint unit has been programmed by the user to break on specific conditions or sequences of events. At operation 310, the breakpoint unit sends a clock freeze signal to the bus arbiter. The bus arbiter then stops granting requests for the bus at operation 315. At operation 320, the bus arbiter checks for any pending operations on the bus. If there are pending operations on the bus, the bus arbiter checks to see if they are complete in operation 325. If they are not complete, the arbiter continues to monitor. If the arbiter finds that they are complete in operation 330, the arbiter then sends the qualified clock freeze signal to the CSL clock and the system is frozen. At this point, because there are no further transactions pending, there will be no wait state generated. Therefore the problem of freezing the system in a wait state is avoided. The user may now access the system from the bus and continue with debugging through the JTAG debugging port.

The process of the present invention may be implemented through use of a machine-readable medium that includes any mechanism that provides (i.e. stores and/or transmits information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method comprising:

ceasing bus access, in a configurable system on a chip, upon the occurrence of a specified event;

allowing completion of all pending bus transactions;

stopping the system clock such that the state of the hardware is held static; and

accessing the static state of the hardware through a debug port.

2. The method of claim 1, wherein the bus is a pipeline bus.

3. The method of claim 1, wherein the debug port is a bus master.

4. The method of claim 1, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions.

5. The method of claim 4, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions.

6. The method of claim 1, wherein the specified event is programmed by a user.

7. A machine-readable medium that provides executable instructions, which when executed by a processor, cause said processor to perform a method comprising:

ceasing bus access, in a configurable system on a chip, upon the occurrence of a specified event;

allowing completion of all pending bus transactions;

stopping the system clock such that the state of the hardware is held static; and

accessing the static state of the hardware through a debug port.

8. The machine-readable medium of claim 7, wherein the bus is a pipeline bus.

9. The machine-readable medium of claim 7, wherein the debug port is a bus master.

10. The machine-readable medium of claim 7, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions.

11. The machine-readable medium of claim 10, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions.

12. The machine-readable medium of claim 7, wherein the specified event is programmed by a user.

13. An apparatus comprising:

means to cease bus access, in a configurable system on a chip, upon the occurrence of a specified event;

means to allow completion of all pending bus transactions;

means to stop the system clock such that the state of the hardware is held static; and

means to access the static state of the hardware through a debug port.

14. The apparatus of claim 13, wherein the bus is a pipeline bus.

15. The apparatus of claim 13, wherein the debug port is a bus master.

16. The apparatus of claim 13, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions.

17. The apparatus of claim 16, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions.

18. The apparatus of claim 13, wherein the specified event is programmed by a user.

ABSTRACT

A scheme for freezing the clock of a CSOC to obtain a static view of the hardware for debugging purposes. A breakpoint unit is programmed to break on specific conditions or sequence of events. The breakpoint unit monitors the bus. Upon the occurrence of the programmed event the breakpoint unit generates a clock freeze signal. The clock freeze event signal is input to the bus arbiter which causes the bus arbiter to stop granting access to the bus to any bus master except the debug port. The bus arbiter checks for pending transactions on the bus and monitors the completion of any pending transactions. This ensures that the system will not be frozen while in a wait state which would render the bus inoperable. Once all pending transactions are complete, the bus arbiter generates a qualified clock freeze signal to the CSL clock thereby freezing the system for debugging.

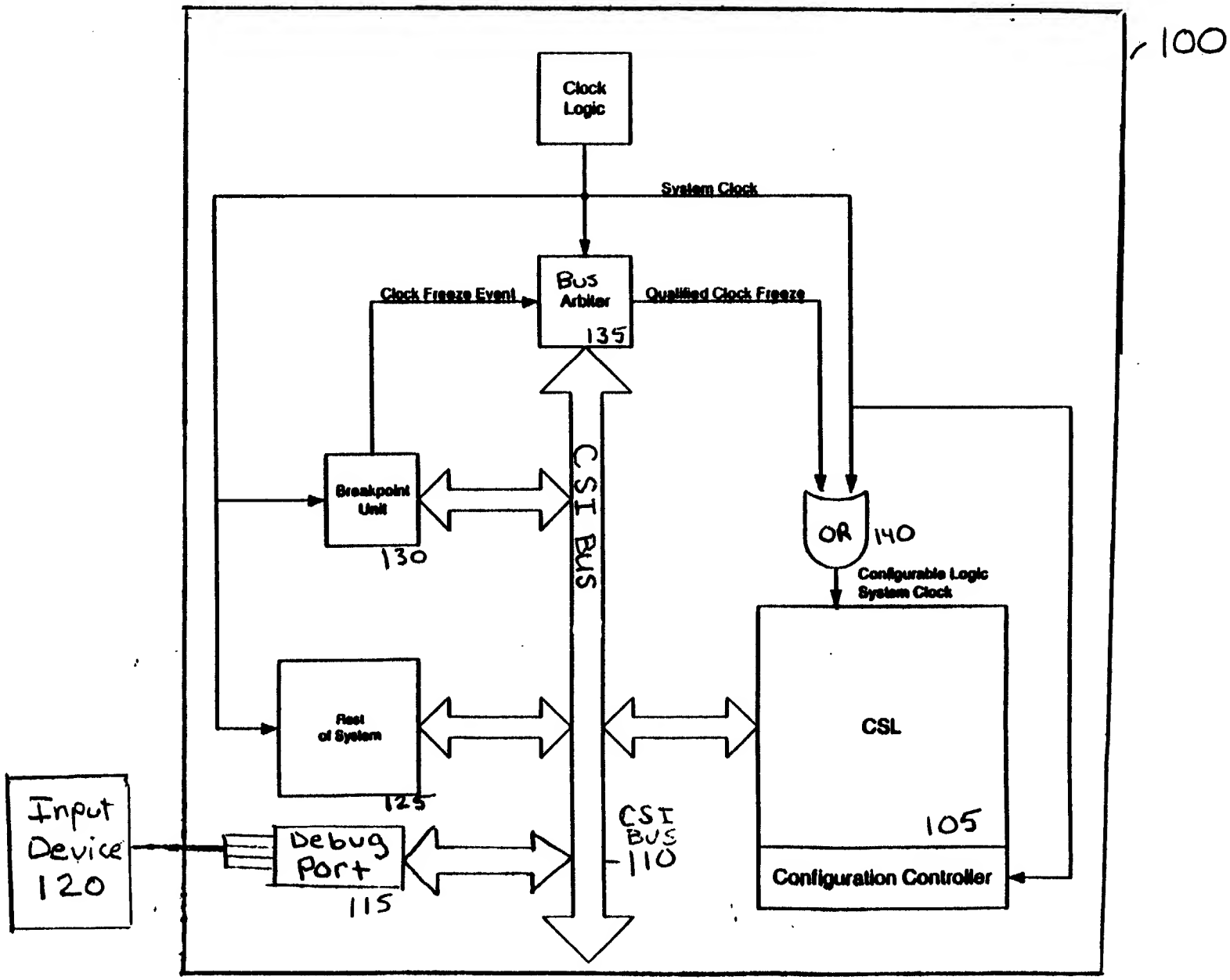

Fig. 1

CSOC Block Diagram

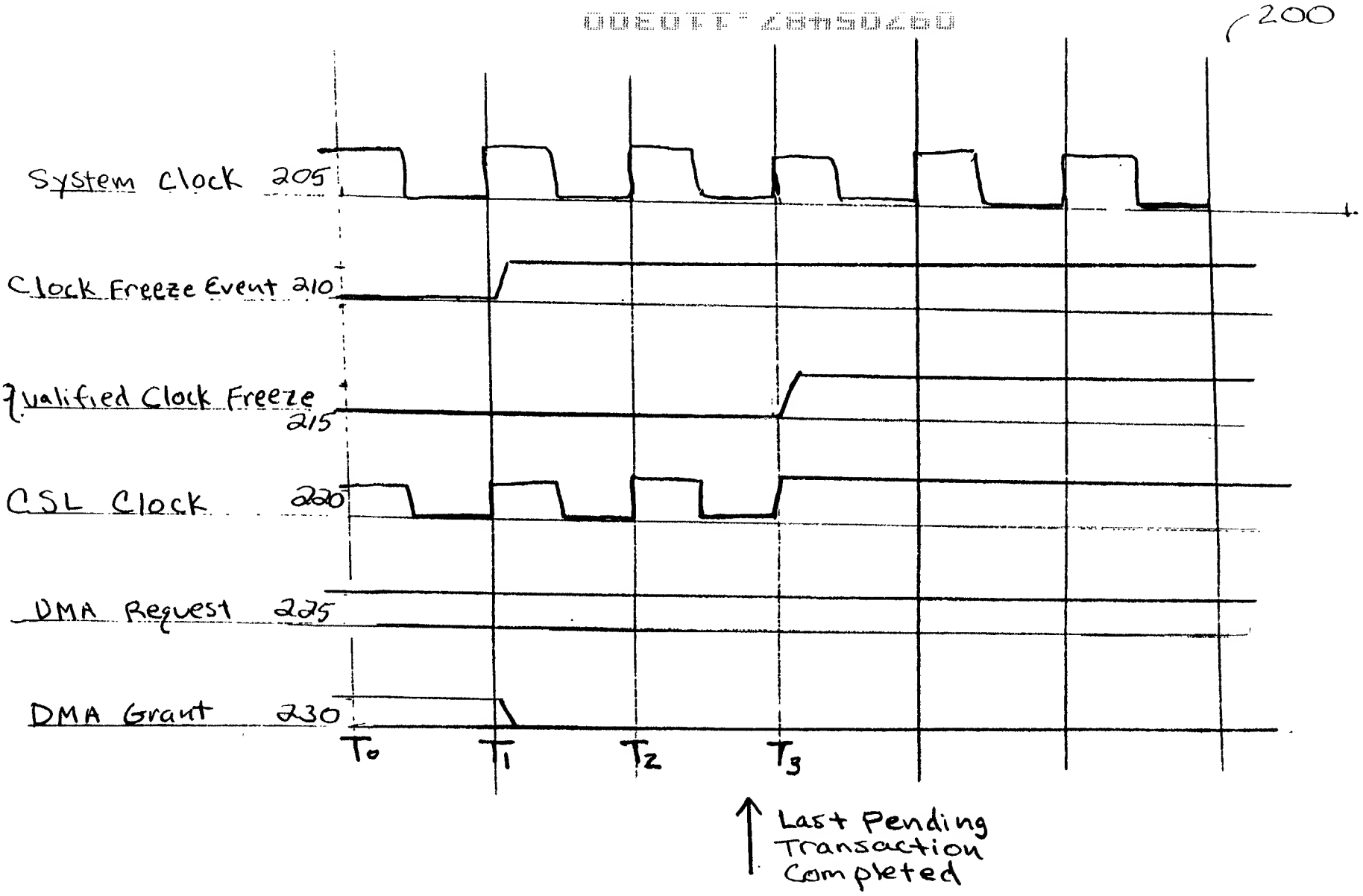

Fig. 2

Clock Freeze Timing Diagram

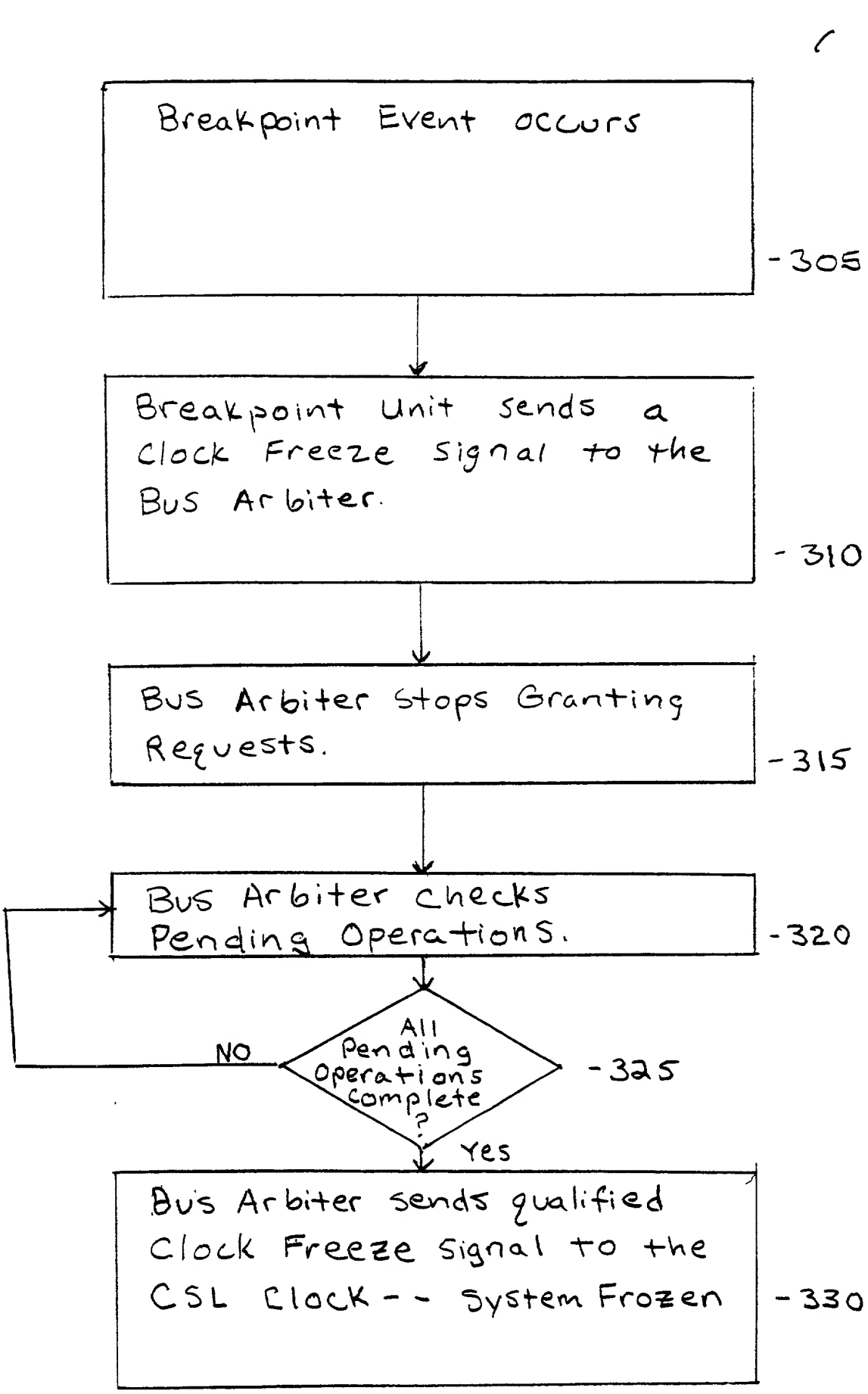
300
Breakpoint Event occurs
305
Breakpoint Unit sends a Clock Freeze signal to the Bus Arbiter.
310
Bus Arbiter Stops Granting Requests.
315
Bus Arbiter checks Pending Operations.
320
All Pending Operations Complete ?
NO
325
Yes
Bus Arbiter sends qualified Clock Freeze signal to the CSL Clock -- System Frozen
330

Fig. 3